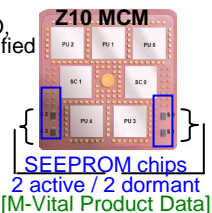


CheatSheet

#50 zTidBits

z10 RAS

Reliability Availability Serviceability



- The IBM System z10 platform continues the System z mainframe institution of delivering the optimum level of system RAS.
 - With every new generation, a noteworthy number of innovative RAS functions and features are introduced, and the z10 platform is no exception.
 - [This issues describes a small number of new details on hardware and firmware].
- Many profile and configuration changes made under PR/SM are now fully concurrent and the need to preplan for future growth requirements was removed by making following actions fully concurrent:
 - Adding logical processors to a partition.
 - Adding a cryptographic adjunct processor to an LPAR.
 - Adding logical partitions (LPARs).
 - Enabling dynamic I/O.
 - Adding logical I/O channel subsystems (LCSSs).
 - Adding "logical device" subchannel sets (subchannel = logical device)

- As increases were made in the performance of each processor, the total number of processors, the total size of the memory, the amount of cache, the bandwidth of the I/O, the thermal density, and the exposure to soft errors with these changes demanded fortified RAS functions to prevent unscheduled outages.
- The dependability of the z10 platform was enhanced extensively as a result of the level of integration possible with CMOS 11S SOI (silicon-on-insulator) technology.
- The number of chips on the multichip module (MCM) was condensed to 7 chips, from 16 on the z9 MCM (this offers less moving parts for something to go wrong).
- The z10 processor chip now supports single-core **checkstopping** and transparent CPU (central processing unit) sparing.
 - A reduced soft-error rate first-level packaging approach is now used on the MCM.
 - Now hard errors are handled by checkstopping the processor and moving the task to a spare processor, where processing then continues.
 - > The identity of the processor is virtualized so that moving the task is transparent to the application (z9 used a SAP as transient PU until new processor was made available).
- Two spare processors are provided on all z10 models, but any unassigned processor will also be used as a spare.
 - Unlike the z9 system, the z10 system can checkstop and spare each core individually.
 - The PU book will be called for replacement on the third transparent CPU sparing event.
 - [The book can be replaced concurrently on servers with two or more books]

NOTE: Checkstopping is when a processor has a known logic failure. The reliability strategy is to stop using the core processor, which includes the interface with the L2 cache, as such, abruptly discontinue processing by 'stopping' the clocks and moving the task to a spare processor, where task execution then continues.

[New microarchitecture state information has been introduced into the z10 chip design]

- The architectural machine state is saved under strong **error-correcting code (ECC)** at instruction checkpoints.
 - The detection of an error causes the checkpoint state to be restored, the caches to be purged, and the instruction to be retried.

NOTE: The z10 does not employ instruction mirroring as in past chip designs. When extensive duplication is used, the recovery unit design and simulation become limiting factors in the processor design. The z10 platform would have approached the limit of this design, and the decision was made to use traditional inline checking using traditional parity, that is, checking function by function rather than using massive duplication which reduces the size of the recovery unit.

- The new z10 **3-MB level 1.5** cache per core is a parity protected store-through cache, similar to the level 1 cache.
 - Hard errors found while running are tolerated by what's called a compartment delete (a compartment is one twelfth of the cache). The cache can permanently relocate the hard errors using a spare cache array where the relocation of the data for each core is stored in the **SEEPROM (serial electrically erasable programmable read-only memory)** on the MCM.
 - The SEEPROM data is formatted according to the MCM-specific data, and referred to as the **Vital Product Data (VPD)**.

- The z10 processor chips are tested at elevated temperature and voltage during the manufacturing process to accelerate any failures and thereby remove the weakest chips from the product.
 - Here is where MCMs have 17 v.s. 20 CPs installed depending on machine model.
 - Elevating the temperature and voltage places the chip at the limits of its test tooling.
 - Voltage islands were introduced on the processor chip to allow manufacturing relief during testing.
 - Each core is powered separately, and the voltage of one core can be stressed while the other cores remain at nominal.
 - Normally, z9 manufacturing variability allowed that one chip may be faster while another may be slower.
 - > This variability is typically mitigated by screening to a lowest common denominator or by sorting chips into different product lines.
 - The z10 solution is different where each processor chip is provided a custom voltage level.
 - >Each chip is tested in manufacturing, and an optimum voltage is selected.
 - >The voltage setting for each chip is also stored in the VPD for the MCM, which allows for unique operating conditions on an individual chip basis. VPD is also referred to as the **Module-VPD (M-VPD)**.

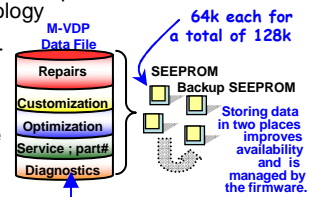
ECC: Error-correcting code is an algorithm for expressing a sequence of numbers such that any errors which are introduced can be detected and corrected (within certain limitations) based on the remaining numbers.

- A consolidated **z10 M-VPD** architecture was introduced to store the broad range of chip 'health' information that is now contained on the MCM itself.
 - The z9 system and prior generations allowed only soft fuses, known as **eFuses**, to store information in a chip or module.
 - However eFuses can be written only once inhibiting repairs if a failure is found.
 - Z10 generation of chips being more difficult to manufacture than previous generations because of increased circuit density, design complexity, and manufacturing variations and, therefore, requires more flexibility than was previously available with the soft fuse approach.
 - M-VPD gives manufacturing the ability to customize each chip, thereby enabling a wider criterion to manage yield without having to use complex part numbering.
 - Manufacturing for z10 chips stores custom information about arrays, interfaces, optimum electrical energy levels, and the number of functional cores.
 - Each server uses this stored information to customize chip usage providing the customer with a cost-effective solution without compromising reliability or performance
 - The data is written into the M-VPD array now making it possible to update the array in order to repair any data.
 - The **field replaceable unit (FRU)**-repair field in M-VPD contains information necessary for repair actions on the book (that includes the MCM) and is used by the Support Element.
 - This repair process now adds more data to the M-VPD file to aid in diagnosing the cause of the part for replacement.

NOTE: The limited number of eFuses requires that the repair data be stored in a simple fixed record format. M-VPD allows data to be stored in longer records of varying length with context-specific formats. This allows for records that are optimized for efficient processing, which improves the initial machine load or the reboot for performance.

- The M-VPD architecture allows for generalized validity checking and error correction of all records allowing chip designers to place critical chip-specific data on the MCM along with the chips.
- The introduction of four processor cores on a single chip is a challenge to manufacturing
 - One core may be defective while the other three are operational.
 - The z10 system has two part numbers: one for a system with 17 active cores and one with 20 active cores.
 - Both MCMs have five processor chips; however, not all cores are active on the former
 - Because manufacturing manages its supply and demand on a part-numbers basis, M-VPD provides an efficient method for managing their requirements.
 - SEEPROM located on the MCM is read-write technology and written as needed.

- To match the high reliability design of these processor chips a redundant SEEPROM is used and therefore redundancy is complete from SEEPROM through the storage controller (SC) L2 cache.
- The FRU is used by IBM to dispatch, if necessary the correct replacement part for the Book.
- The FRU is also used by the support element (SE) to direct technicians through the repair process.
 - The repair process adds more data to the M-VPD to aid in diagnosing the causing of the part replacement.



•**Three possible cases** that can result in problems with SEEPROM, the Support Element (SE) or any path between them are:

1. While updating a SEEPROM (physically two SEEPROMs).
 - [Firmware handles this by managing an update-in-progress flag in each SEEPROM]
2. After updating one SEEPROM and before the other.
 - [This occurs after the update-in-progress flag is cleared in the first SEEPROM creating a consistent copy of the data where the data from the first SEEPROM is brought over to the second SEEPROM].
3. Before storing data (...having a defective SEEPROM).
 - [In this case, the SEEPROM is not replaced for one faulty component. This is where M-VPD implements the backup support records in the alternate SEEPROM.
 - Note:** The backup record is always written prior to writing the primary record. The original record is unaltered when a failure occurs while writing the backup record. BUT, conversely, the backup record is available if a failure occurs while writing the primary record. A write failure can be detected on a read by the ECC algorithms].

eFuse adds the equivalent of numerous tiny electrical fuses to each chip that, when combined with special onboard software, can allow the chips to alter their own internal circuitry to circumvent problems, but are fixed in size and as well as function.