



Models (2097)	Processor Units CMOS 11S (4.4GHz)	Memory	InfiniBand Connections	I/O Cages	Maximum Channels
E12	1 to 12	16 to 352* GB	16	1 to 3	960
E26	1 to 26	16 to 752 GB	32	1 to 3	1024
E40	1 to 40	16 to 1136 GB	40	1 to 3	1024
E56	1 to 56	16 to 1520 GB	48	1 to 3	1024
E64	1 to 64	16 to 1520 GB	48	1 to 3	1024

z10 Enterprise Class is offered in five models.

The model naming is representative of the maximum number of customer configurable processor units (PUs) in the system. PUs are delivered in single engine increments orderable by feature code. The model number also reflects the number of books installed. The z10 EC models, corresponding feature codes, and maximum number of books allowed are:

- IBM Model E12 (FC 1117) - One book
- IBM Model E26 (FC 1118) - Two books
- IBM Model E40 (FC 1119) - Three books
- IBM Model E56 (FC 1120) - Four books
- IBM Model E64 (FC 1121) - Four books

• Conversion of CPs, IFLs, zIIPs or ICFs to and from zAAPs
• z/OS 1.9 will support up to 54 engines in a single LPAR

The z10 EC is designed and optimized for growth and large scale consolidation. The z10 EC provides:

- Up to 64 customer processor units (PUs)
- Up to 384 GB of memory per book (4 book max)
 - z9 uses 128 GBs per book
- Up to 1.5 TB of total available machine memory (z9 has 512 GB)
- Up to 12 PUs available for subcapacity use (z9 has 8)
- Up to 60 LPARs

InfiniBand connections use internal I/O with a link rate of 6 GBps (CF- 2Q2008) - z9 link rate is 2.7 GBps STI.

Power estimating and monitoring functions:

- Power Estimator tool on Resource Link -

Monitoring of power consumption and thermal loading on the Activity task on the Hardware Management Console. Support for IBM Systems Director Active Energy Manager for x86, IBM Systems Director Active Energy Manager for POWER and IBM Systems Director Active Energy Manager for Linux on System z (available 2Q2008), which can monitor power and thermal data for z10 EC, as well as other systems.

Capacity on Demand functions, which include:

- Ability for a permanent LIC-CC upgrade when temporary resources are active
- Ability to install and activate multiple temporary records at any given time
- Ability to activate partial resources on a single temporary record
- Disaster recovery solutions:
 - > Capacity for Planned Events (CPE) - Short range - 3 days
 - > Capacity Backup (CBU) - Long range - 90 days
- Capacity provisioning, which provides a means of managing your processing capacity based on business needs
- 36 available subcapacity settings.

HiperDispatch helps provide increased scalability and performance of higher n-way and multibook System z10 systems by improving the way workload is dispatched across the server. HiperDispatch accomplishes this by recognizing the physical processor where the work was started and then dispatching subsequent work to the same physical processor. This intelligent dispatching helps reduce the movement of cache and data, and improves CPU time and performance.

Reduced impact of Planned and unplanned outages

- Enhanced Book availability
- Redundant I/O interconnect
- Enhanced Driver maintenance
- Dynamic oscillator switch over

*16 GB dedicated HSA on the z10 EC

- High frequency quad-core processor
- 4 cores per die: 3MB private on L1.5 cache
- Hardware accelerators on chip for:
 - data compression
 - cryptographic functions
 - hardware decimal floating point (HDFU); big boost for Java/ C/C++ and financial transaction throughput; previously done through software libraries; z10 provides greater support for CPU-intensive workloads i.e. RISC type workloads)
- New optional 1MB Page Frame via z/OS 1.9 (previous 4k)
- 64-bit I/O architecture for CCW indirect data addressing to designate data addresses above 2GB for format-1/-2 CCWs (big I/O boost)
- 50+ instructions added to z10 Chip improving compile code efficiency *Big performance boost!*
- New L1/L1.5/L2 cache hierarchy design – cache is fully connected (dual ring in z9)
- Flexible Memory provides the additional resources to maintain a constant level of storage
- Infiniband connections 2x data transfer rate increase (6GBps) over z9 using STI (2.7GBps) (This uses a switch fabric communication link)
- Rich CICS Instruction Set Architecture (ISA)
- Multi-address space robust inter-process security
- Capacity Provisioning and WLM (z/OS 1.9); When the defined conditions are met, z/OS can add or remove temporary capacity automatically with no operator intervention (On/Off CoD)
- The Logical Channel Subsystem (LCSS) allows you to install more operating system images up to 1024 channels (256 max per OS) allowing each z10 access to more I/O and networking channels, links and adapters.
- CP Assist Cryptographic Functions (CPACF) delivers cryptographic support on every PU with enhanced data encryption / decryption (AES 128/192/256bit keys, SHA-1/256/384/512 msg digest, PRNG, DES and TDES)
 - Dynamically add, move or delete Crypto Express2 to or from LPAR
- FICON Express4 offers 2 unrepeatable distance options 4KM and 10KM supporting 4Gbps link data rate with auto-negotiation
- OSA-Express3 10 GbE Long Reach (LR) (2Q2008) doubles the port density using a single I/O slot
- z/VM V5.2 and V5.3 provide support for System z10:
 - Compatibility support for z/VM V5.2 and V5.3 is provided with PTFs.
 - z/VM V5.2 and V5.3 with PTFs allow guests to exploit the System z10 EC at the System z9 functionality level.
 - Exploitation of selected functions of the System z10 include dynamically adding processors to or removing processors from a z/VM LPAR
- Unsupported on z10: OSA-EXPRESS, PCIXCC/PCICA, ICB-2/-3, ISC3 in compatibility mode
- Upgrade availability from z990 or System z9 to z10 EC.

Model Capacity Indicator = 7xx, 6xx, 5xx, 4xx where xx is the # of active CP features
 - 7xx is a full capacity identifier (i.e. 712 = E12)
 - 6xx, 5xx and 4xx are subcapacity
 - Ex. 510 equals 10 active at CP5 capacity
 - LSPR will reference 701 – 764 model names